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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/679,377	10/07/2003	Dong Suk Shin	40296-0038	4288

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EXAMINER	
CHEN, KIN CHAN	
ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 06/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 10/679,377	**Applicant(s)** SHIN, DONG SUK
	Examiner Kin-Chan Chen	**Art Unit** 1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *092404*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

U.S. Patent and Trademark Office
PTOL-326 (Rev. 1-04) **Office Action Summary** Part of Paper No./Mail Date 061605

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> **(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.**

3. Claims 1-4 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by admitted prior art.

Admitted prior art (page 2, line 15 to page 3, line 23) discloses a conventional method. A buffer layer and an interlayer insulating film may be formed sequentially on a semiconductor substrate. The interlayer insulating film and the buffer layer may be etched to form a contact hole exposing the semiconductor substrate. A cleaning process of a lower portion of the contact hole may be performed. An impurity may be doped into the surface of the semiconductor substrate exposed by the contact hole. The contact hole may be filled with a conductive layer. The buffer layer may comprise nitride, and the interlayer insulating layer may comprise an oxide film. The cleaning process may comprise dry cleaning and wet cleaning. The doping may be performed by ion-implanting.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 9-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art.

The above-cited claims differ from the admitted prior art by specifying well-known features (such as implanting P or As in claim 9; using pH_3 /N_2 to diffuse P in claim 10) to the art of semiconductor device fabrication and using various compositions, processing parameters (such as claims 11-15; 17, 18). However, same were known to be result effective variables and commonly determined by routine experiment. The process of conducting routine experimentations (optimizations) so as to produce an expected result is obvious to one of ordinary skill in the art. A person having ordinary skill in the art would have found it obvious to modify admitted prior art by performing routine experiments (by using various compositions and different processing parameters) to obtain optimal result and adding any of same well-known features same in order to provide their art recognized advantages and produce an expected result.

Dependant claim 16 differs from the prior art by specifying various sizes / dimensions (e.g., thickness of a layer). Because same are merely a matter of choices of design depending on the product requirements, it would be obvious to one skilled in the art to use various dimensions for fabricating a semiconductor device in order to accommodate the specific product design and meet the product requirement.

6. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art in view of Hineman et al. (US 6,372,657) and Ngo et al. (US 6,436,808).

Admitted prior art (page 2, line 15 to page 3, line 23) discloses a conventional method. A buffer layer and an interlayer insulating film may be formed sequentially on a semiconductor substrate. The interlayer insulating film and the buffer layer may be etched to form a contact hole exposing the semiconductor substrate. A cleaning process of a lower portion of the contact hole may be performed. An impurity may be doped into the surface of the semiconductor substrate exposed by the contact hole. The contact hole may be filled with a conductive layer.

Unlike the claimed invention, admitted prior art does not teach using the claimed plasma of the mixture gas for dry cleaning. In a method of cleaning the opening (contact holes) of insulating layer, Hineman (abstract) teaches that a cleaning gas may comprise NH_3 and oxygen, and Ngo (col. 3, line 53 through col. 4, line 6) teaches that a cleaning gas may comprising NH_3 and N_2 in order to efficiently clean the opening (contact holes) before filling the conductive material. Hence, it would have been obvious to one with ordinary skill in the art to use NH_3, N_2, and oxygen to cleaning the opening (contact holes) of insulating layer in the process of the admitted prior art in order to efficiently clean the opening (contact holes) before filling the conductive material. Furthermore, it would have been obvious to one with ordinary skill in the art to use to add inert gas (e.g., Helium) in the etching /cleaning gas in order to improve the uniformity of cleaning and stabilizing the cleaning process. *Incorporation of a carrier or diluent was held to have been obvious. In re Lerner 169 USPQ 51 (CCPA 1971); In re Rosicky 125 USPQ 341 (CCPA 1960).*

Dependent claims 5 and 6 differ from the combined prior art by specifying well-known features (such as annealing in claim 6) to the art of semiconductor device fabrication and using various processing parameters (such as claims 5 and 6). However, same were known to be result effective variables and commonly determined by routine experiment. The process of conducting routine experimentations (optimizations) so as to produce an expected result is obvious to one of ordinary skill in the art. A person having ordinary skill in the art would have found it obvious to modify admitted prior art by performing routine experiments to obtain optimal result and adding any of same well-known feature to same in order to provide their art recognized advantages and produce an expected result.

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art in view of Ha et al. (US 6,369,008).

Admitted prior art (page 2, line 15 to page 3, line 23) discloses a conventional method. A buffer layer and an interlayer insulating film may be formed sequentially on a semiconductor substrate. The interlayer insulating film and the buffer layer may be etched to form a contact hole exposing the semiconductor substrate. A cleaning process of a lower portion of the contact hole may be performed. An impurity may be doped into the surface of the semiconductor substrate exposed by the contact hole. The contact hole may be filled with a conductive layer.

Unlike the claimed invention, admitted prior art does not teach using the claimed solution for wet cleaning. In a method of cleaning the opening (contact holes) of insulating layer, Ha discloses that a wet cleaning solution may be HF, H_2O_2, or ammonium hydroxide in order to remove etching by product and damaged film resulting therefrom. See abstract, col. 1, lines 34-42; col. 4l lines 15-34. Hence, it would have been obvious to one with ordinary skill in the art to use a wet cleaning solution of HF, H_2O_2, or ammonium hydroxide to clean the opening (contact holes) of insulating layer in the process of the admitted prior art because Ha teaches that to do so will remove etching by product and damaged film.

8. Claims 1-4 and 8-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung et al. (US 6,562,651).

In a method of manufacturing a semiconductor device, Chung teaches that a silicon nitride (so-called buffer layer in instant claims) and an interlayer insulating film may be formed sequentially on a semiconductor substrate. The interlayer insulating film and silicon nitride may be etched to form a contact hole exposing the semiconductor substrate. A cleaning process of a lower portion of the contact hole may be performed. An impurity may be doped into the surface of the semiconductor substrate (e.g., source /drain region). The contact hole may be filled with a conductive layer. See col. 1; 30-67; col. 3 and 4; Figs. 6 and 10. The claimed invention differs from Chung by stating doping impurity after forming the contact hole rather than doping impurity before forming the contact hole. However, Since the method of Chung produces doped (ion-implanted) surface of the semiconductor substrate that exposed by the contact hole, and cleaning the contact holes, filling the contact hole with conductive layer thereafter, which are considered to produce the same structure and achieve the same purpose of reducing contact resistance as instantly claimed.

Changes in sequence of processing steps and the selection of any order of performing process steps are prima facie obvious in the absence of new result. Ex parte Rubin, 128 USPQ 440. See also In re Burhans, 154 F.2d 690, 69 USPQ 330.

The above-cited claims differ from Chung by specifying well-known features (such as implanting P or As in claim 9; using pH_3 /N_2 to diffuse P in claim 10) to the art of semiconductor device fabrication and using various compositions, processing parameters (such as claims 11-15; 17, 18). However, same were known to be result effective variables and commonly determined by routine experiment. The process of conducting routine experimentations (optimizations) so as to produce an expected result is obvious to one of ordinary skill in the art. A person having ordinary skill in the art would have found it obvious to modify admitted prior art by performing routine experiments (by using various compositions and different processing parameters) to obtain optimal result and adding any of same well-known features same in order to provide their art recognized advantages and produce an expected result.

Dependant claim 16 differs from the prior art by specifying various sizes / dimensions (e.g., thickness of a layer). Because same are merely a matter of choices of design depending on the product requirements, it would be obvious to one skilled in the art to use various dimensions for fabricating a semiconductor device in order to accommodate the specific product design and meet the product requirement.

9. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung et al. (US 6,562,651) as applied to claims 1-4 above, and further in view of Hineman et al. (US 6,372,657) and Ngo et al. (US 6,436,808).

The discussion of modified Chung from above is repeated here.

Unlike the claimed invention, Chung does not teach using the claimed plasma of the mixture gas for dry cleaning. In a method of cleaning the opening (contact holes) of insulating layer, Hineman (abstract) teaches that a cleaning gas may comprising NH_3 and oxygen, and Ngo (col. 3, line 53 through col. 4, line 6) teaches that a cleaning gas may comprising NH_3 and N_2 in order to efficiently clean the opening (contact holes) before filling the conductive material. Hence, it would have been obvious to one with ordinary skill in the art to use NH_3, N_2 and oxygen to cleaning the opening (contact holes) of insulating layer in the process of Chung in order to efficiently clean the opening (contact holes) before filling the conductive material. Furthermore, it would have been obvious to one with ordinary skill in the art to use to add inert gas (e.g., Helium) in the etching /cleaning gas in order to improve the uniformity of cleaning and stabilizing the cleaning process.

Incorporation of a carrier or diluent was held to have been obvious. In re Lerner 169 USPQ 51 (CCPA 1971); In re Rosicky 125 USPQ 341 (CCPA 1960).

Dependent claims 5 and 6 differ from the combined prior art by specifying well-known features (such as annealing in claim 6) to the art of semiconductor device fabrication and using various processing parameters (such as claims 5 and 6). However, same were known to be result effective variables and commonly determined by routine experiment. The process of conducting routine experimentations (optimizations) so as to produce an expected result is obvious to one of ordinary skill in the art. A person having ordinary skill in the art would have found it obvious to modify the combined prior art by performing routine experiments to obtain optimal result and adding any of same well-known feature same in order to provide their art recognized advantages and produce an expected result.

10. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chung et al. (US 6,562,651) as applied to claims 1-4 above, and further in view of Ha et al. (US 6,369,008).

The discussion of modified Chung from above is repeated here.

Unlike the claimed invention, Chung does not teach using the claimed solution for wet cleaning. In a method of cleaning the opening (contact holes) of insulating layer Ha discloses that a wet cleaning solution may be HF, H_2O_2, or ammonium hydroxide in order to remove etching by product and damaged film resulting therefrom. See abstract, col. 1, lines 34-42; col. 4, lines 15-34. Hence, it would have been obvious to one with ordinary skill in the art to use a wet cleaning solution of HF, H_2O_2, or ammonium hydroxide to cleaning the opening (contact holes) of insulating layer in the process of Chung because Ha teaches that to do so will remove etching by-product and damaged film.

Claim Objections

11. Claim 5 is objected to because of the following informalities:

In claim 5, line 3, "HE" should read – He -- or –helium–.

Appropriate correction is required.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kin-Chan Chen whose telephone number is (571) 272-1461. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571) 272-1465. The fax phone number

for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 16, 2005

K. Chen

Kin-Chan Chen
Primary Examiner
Art Unit 1765